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INSURANCE FOR SEMICONDUCTOR PLANTS DURING CONSTRUCTION AND OPERATION

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Introduction

With the ever-increasing demand for the supply of integrated circuits (IC) (see slide 3, Introduction), the semiconductor industry has seen unparalleled growth rates. The extreme requirements for the manufacturing of IC's in specialised production facilities (herein referred to as "fabs") have created exposures to insurers that have often been underestimated in the past. Large losses have confirmed semiconductor fabs' huge loss potential. This paper is intended to point to the specific exposures insurers face when insuring semiconductor fabs and to offer ideas for adequate insurance concepts. A thorough understanding of the manufacturing processes is essential to raising awareness of the specific risk characteristics of fabs. Therefore, the paper also attempts to describe the technology and core processes being used in the semiconductor industry.

Introduction

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top of main document

Semiconductor Industry

1. Semiconductor Fabs

Semiconductor fabrication facilities, or "fabs", are the centers of high volume complex manufacturing in the semiconductor industry. Typically, a fab is a building that contains offices, locker rooms, storage facilities, test and packaging rooms and other support spaces. At the heart of every fab is the clean room (see slide 4): a sealed, pure environment with less than one particle of dust, no larger than 0.5 micron, per cubic foot of air. As even a single particle of dust can render a good chip useless, every surface and piece of equipment in the clean room is freshly scrubbed and maintained so that it appears brand new: gleaming in the bright, florescent light. There is a constant, low level hum of ure air being pumped in through the ceiling. Workers wear so-called "bunny suits" (i.e., Gore-tex jumpsuits, with face masks, hair caps and rubber gloves) that cover up everything but their safety glasses (see slide 5).

Semiconductor industry

Inside views of a clean room

Semidonductor industry

Typical cross section of a semiconductor lab

Chip fabrication is the primary function of a clean room. Chip fabrication transfers the circuitry, layer by layer, onto silicon wafers. First, mask patterns are etched onto the wafers, which are then coated with materials and treated with dopants to stimulate electronic flow. The total number of "prescribed" steps varies with the complexity of the circuit being built, but completion will often take more than 2 months. Despite the many steps and types of activities undertaken (planarization; cleaning; etching; diffusion; chemical coating; lithography; oxidation; implantation; sputtering; grinding; polishing; chemical vapor deposition; testing; and spinning) only the following three basic operations are performed:

- coating thin layers of insulators, semiconductors, conductors, photoresist or other materials onto wafers using thermal oxidation, vapor deposition, evaporation, or

sputtering methods;
- removing selective portions of the thin layers to form patterns. The masks control the exposure of a photoresist layer to ultra-violet light, e-beams or x-rays. Exposed parts are etched from the silicon wafer to form the desired patterns;
- doping wafers to induce electronic flow using thermal diffusion or ion implantation techniques.

The fabrication process produces integrated circuits or "chips" worth billions of dollars. A single chip can contain millions of transistors. Hundreds of different steps are required to complete the process - some requiring very high temperatures (higher than 800 *C) and all involving almost inconceivably small features. Some of them, for example, measure less than a micron in width, a single human hair being roughly 50 microns in diameter. The resulting product often features more than 300 thumbnail-size chips on a 200mm (8 inch) wafer. Due to the value of each individual chip, the value of one wafer may exceed hundreds of thousands of dollars.

Chip fabrication is increasingly moving toward smaller circuits and more transistors per chip at a rate that doubles the transistor density every 18 to 24 months (Moore's Law). To this end, specialists continue to evaluate ways to obtain:

- larger wafer size,
- smaller size circuits,
- more layers of circuits per wafer,
- new materials,
- new processes, and
- more integrated process automation.

These characteristics of the chip production process have resulted in stringent requirements in respect of quality, reliability and precision in all production steps (see slide 6, Yield of Semiconductor Production).

Semiconductor industry	
Yield 8output) of Semidoncuctor production on the basis of a production process with 400 steps	
Yield per step (%) / Total yield (%)	
98.00 / 00.03	
99.00 / 01.00	
99.50 / 13.50	
99.95 / 81.90	
99.99 / 96.00	

The yield or output (and thus the profitability) of semiconductor production is highly sensitive to even very small variations in the individual productions steps (see slide). Since the majority of the production equipment has to meet extreme requirements in terms of precision and quality standards, it is generally very expensive and also highly sensitive to

damage due to contamination or improper handling. As such, special considerations need to be applied when setting up insurance terms for this kind of equipment.

top of Semiconductor Industry

top of main document

2. Plant Demographics

The semiconductor industry is truly a global one. During the design-to-market process, each chip will typically travel more miles than most people do in a lifetime! The chip may be designed, for example, in Oregon, USA; the prototype fabricated in a development fab located in California, USA. Later, the high volume production may occur in a fab located in Ireland, with the fab's "virtual factory" being located in Arizona USA. The completed wafer will then be transported to Malaysia for testing, then assembled in the Philippines. Finally, the finished chip will be sent back to either Arizona, USA for distribution or to a board/box plant in Puerto Rico.

Despite the current slow down in the industry, global expansion of the semiconductor industry is forecasted to be exponential in the coming years. The Semiconductor Equipment and Materials International (SEMI) organization predicts that over the next five years the:

- global electronics industry will grow from USD 851 billion to USD 1389 billion (10% growth rate);
- semiconductor industry will grow from USD 135 billion to USD 275 billion (16% growth); (see slide 7)
- semiconductor equipment industry will grow from USD 26 billion to USD 45 billion (12% growth); and
- supply materials industry will grow from USD 19 billion to USD 33 billion (12% growth).

Semiconductor industry

- The fastest growing in the world
- Turnover US$ 135 Bio (1998)
- Estimated growth rate 16% per annum for the next years

Key areas	Market share	Main products
North America	44%	Microprocessors
Japan	36%	Memory chips
Asia ex. Japan	10%	Memory chips
Europe	10%	Application specific chips

To fuel this growth, more and more semiconductor fabs will be required. Semiconductor Equipment and Materials International (SEMI) reports there are 127 new fabs in various stages of planning and construction with total expenditures expected to exceed USD 115 billion. New fabs cost between USD 1.2 and 1.5 billion each! (The new 300 mm fabs may be more than double that cost.) While typically, it takes two to three years to build a new fab, chip product life often does not exceed nine to 12 months.

Geographically, four key areas can be identified. These are:

- North America (Microprocessor production)
- Japan (Memory chip production)
- South East Asia (Memory chip production)

- Europe (Special applications such as ASIC's, Application Specific Integrated Circuits)

Market shares are distributed rather unevenly, with North America (45%) and Japan (35%) taking the lead followed by Europe and South East Asia, whose market shares amount to some 10% each.

top of Semiconductor Industry

top of main document

3. Characteristics

In 1965 Gordon Moore, co-founder of Intel, observed that the number of transistors per square inch on integrated circuits or chips had doubled every year since the invention of the integrated circuit. Moore predicted that this trend would continue for the foreseeable future. In subsequent years, while the pace slowed down a bit, data density has doubled approximately every 18 months in keeping with the current definition of Moore's Law. Most experts, including Moore himself, expect Moore's Law to hold for at least another two decades! The impact of this exponential growth is significant and affects all aspects of the business.

More than most other industries, the semiconductor industry tends to:

- manufacture product at the molecular and sub-molecular level;
- work in an environment 1000 times cleaner than a hospital surgical suite;
- have product changes every nine to 12 months;
- have an historic ability for fast changes;
- work to get its product to market at breakneck speed;
- harbor a strong and continuous improvement philosophy;
- be "virtual" in the truest sense of the word; and
- be extremely complex.

All of the above occurs in semiconductor fabs, which are huge and complicated manufacturing facilities. As the chips get denser with circuits and transistors, the fabs in which they are built also become more complex. Indeed, there is an inverse relationship between the size of the chips and the size and complexity of the plans for their fabs.

How big is big? To build a fab containing a clean room of 8'000 m2 floor area, one easily consumes enough concrete for 25 km of road, 4,500 km of reinforced steel bars, 120 km of ultra clean pipe and 250 km of electrical wire. In addition, one uses enough deionized water (2,000 times cleaner than tap water) to fill 24 swimming pools every day at 150,000 liters per hour, and enough compressed air to fill 3,000 party balloons a minute around the clock. Once the fab is complete, 800 kilowatt hours of electrical energy are consumed to manufacture a single 200 mm (8 inch) semiconductor wafer. That amounts to enough energy to operate a typical household for two months.

top of Semiconductor Industry

top of main document

4. High Cost of Industry

A single fabricated wafer that contains hundreds of chips is worth hundreds of thousands of dollars. A briefcase of chips is worth millions, in turn. Likewise, semiconductor fabs are a major capital investment involving millions of dollars for one piece of wafer-manufacturing equipment or "tool". The total cost of the tools within the fab is equal to, or greater than, the construction and commissioning costs of the fab. Given the volatility of the market, the process to be used in a facility to manufacture the chips is variable - and may even change at the last minute. Given the large investment required, and the uncertainty about the process to be used, it is essential that the equipment is ordered and arrives just-in-time for installation needs.

The pressures on semiconductor manufacturers are mounting. Concerned about worker health and safety, and in the aftermath of fires and explosions, some governments are placing semiconductor operations under closer scrutiny. Research and development costs must be recaptured quickly as companies "leapfrog" ahead of one another with technological innovations. Semiconductor manufacturing firms cannot afford property losses and business interruptions, neither within their facilities nor anywhere
else in their corporate supply chain. Losses, particularly potential intangible losses, which can not be quantified, can undermine reliability. That type of uncertainty can shake investor confidence, affecting shareholder value.

top of Semiconductor Industry

top of main document

5. Rapidly Changing Market

Hi-tech industry is undergoing constant change- even more than other industries. Below are some of its areas which are most markedly affected:

Telecommunications
For the past decade, the semiconductor industry has been relatively easy to understand: in the beginning, there was Intel, and then there was everyone else. Several more recent developments are changing that hierarchy. For the past three years, the growth of chips devoted to handling communications - Internet
access, data transmissions, wireless and land-based phone calls - has exceeded the growth of chips designed for PCs. Cellular phones, routers, set-top boxes, and modems are using up more and more silicon, opening up opportunities to other firms.

300 mm
In the next few years, many companies will retrofit their fabs in order to produce 300 mm (12 inch) silicon wafers, replacing the current 200 mm (8 inch) size. The move from 200 mm wafers to 300 mm wafers is being billed as the "largest industrial transition in history" by the Semiconductor Equipment and Materials International (SEMI) and an expected cost of more than USD 14 billion has been forecasted. However, the limited availability of production tools has meant that the transition from 200 mm to 300 mm was slower than anticipated.

Back End / Front End
Moving back end (also known as "assembly/test") and front end (or "wafer fabrication") operations closer together geographically makes more sense today, many industry managers believe, because backend rules are changing. New levels of factory-wide automation are becoming available to chip assembly shops, and pressure is growing to slash delivery times to customers around the world. At the same time, the nature of chip assembly work is changing as the industry migrates to complex integrated circuit packaging technologies and fab-like environments for advanced back end production gear. Recent improvements, both in equipment automation and factory-wide material handling systems, now make it possible to locate backend chip plants nearly anywhere in the world, regardless of labor costs.

Foundry
More and more startup firms are kicking off without any manufacturing capacity. These firms depend on the foundry business, i.e. on semiconductor fabs producing chips according to the design and specifications developed by specialised companies. Demand for new foundry capacity has grown and will continue to grow. This is evident in the fabless growth rate, which has far outpaced the rest of the industry a few consecutive years. Foundries are becoming the hub of technology driving system level integration. Such foundry manufacturing, mostly in Taiwan, is transforming the chip business
from an oligarch of companies capable of building billion dollar chip plants to an eclectic collection of fabless companies, mostly in the US, that do not own their own factories. As the foundry business takes off, the entry barriers to the semiconductor industry will be lower and the price of failure will not be as great as before.

top of Semiconductor Industry

top of main document

Phases of Fab Development

Typically the product life of a semiconductor chip (nine to 12 months) is less than the time required to construct the facility and install the equipment for manufacturing (24 to 36 months). As such, the construction/commissioning process is a rapid, constantly overlapping and complex set of events. In addition, construction of semiconductor facilities is very complex and costly (about USD 1.2 to 1.5 billion) due to the extraordinarily sophisticated processes and equipment required to manufacture semiconductor chips.

"Moore's Law" rules all aspects of the semiconductor industry, including the facility demands. As a result of "doubling the capacity every 18 months", the need for new or converted facilities seems to be a constant in the industry. Further, the expectation is that these facilities will be built and equipped while meeting breakneck construction timetables. Such intense construction schedules are consistent with the pace of the semiconductor technology, the rush being a result of four phenomena unique to the industry:

- Cut-throat business. The greatest profit margins are realized early in the life cycle and before the competition is up and running; speed in getting to market with the latest product is the bottom line.
- Advancements in technology. These demand a "fast track" approach to getting the capacity up and running that other industries do not need or implement.
- Short product life cycle. This triggers the requirement for an equipped facility early enough to manufacture the product before the next generation of product.
- High cost of the facilities. Without product sales in the near future, the carrying costs are hard to cover.

In traditional construction, a design-then-build method is used. Using this method, the elapsed time from groundbreaking to manufacturing, however, can span three years or longer. Using a "fast-track" or parallel approach to designing and building fabs, however, the process can be completed in less than half that time.

With "fast track" methodology, the owner, architects and contractors work together from the outset, mutually determining and addressing the critical path of the project. In general, the project is broken down into separate "packages", e.g., site work, foundation work, building envelope. Construction begins long before the whole design is complete. Although time is trimmed by this method, the complexity of the process becomes even greater. This also significantly complicates the process of determining ownership.

It is clear that insurance concepts need to reflect the special features inherent to the semiconductor industry. This is particularly true when it comes to warranties in respect of fire precaution measures or the definition of testing and hand-over procedures.

top of main document

Main Hazards in Fab Development and Operation

The threats to semiconductor fabs are numerous (see slide 8).

Main hazards	
• flammable andexplosive gases and liquids • combustible materil • extreme value concentaration • toxic and chemically aggressice media • high temprature	• high voltage • shock sensitivity • corrosion • particle contamination • theft • espionage

They combine traditional exposures common to any production industry with several unique

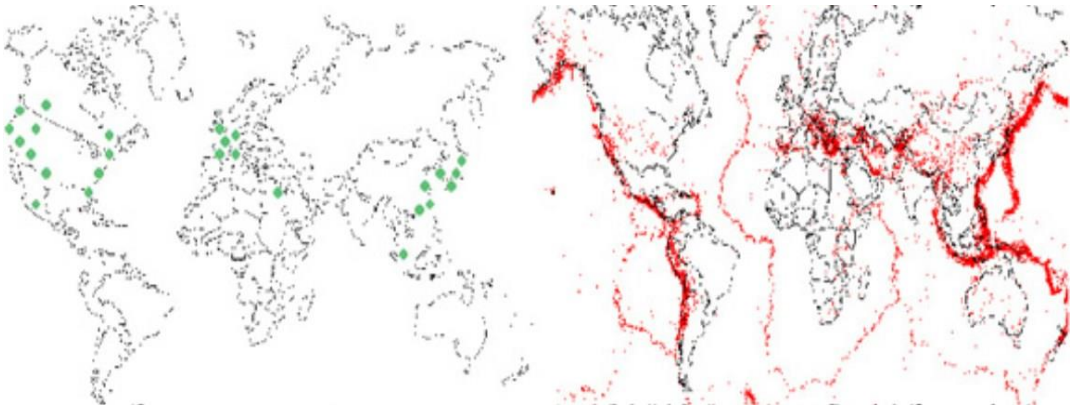
features such as:

- highly flammable/explosive gases and liquids
- use of combustible materials (PP, PVC) for ducts and pipes
- very large fire sections (the entire clean room) with extremely high value concentration
- toxic and chemically aggressive gases and liquids
- high temperature applications
- high voltage apparatus
- shock sensitivity of optoelectronic components
- chemical residue contamination and corrosion
- particle contamination of clean room
- theft
- espionage

The combination of a highly sophisticated and vulnerable production process employing high value machinery and using some of the most aggressive chemicals creates unparalleled challenges for the risk management in semiconductor fabs, as well as for the insurance industry. The assessment and mitigation of potential risk areas are essential for safe operation in any fab and require stringent control of safety procedures on all levels.

Semiconductor fabs need to have special shock-absorbing foundations to shield sensitive machinery from vibrations affecting the quality of the chips. Surprising, then, is that the main manufacturing locations of the semiconductor industry coincide with the main earthquake-prone areas Japan, Taiwan, West Coast of the USA and Central parts of Europe (see slide 9).

Main hazards



Dots represent clusters of up to 10 semiconductor fabs

Earthquake map

Semiconductor activites coincide with eartquake zones

There are approximately 250 semiconductor fabs in operation world wide. Most of them are located in specialised research and development centres or industry parks. The map shows the geographical distribution of these parks. Each dot represents a cluster of up to 10 semiconductor fabs.

Another special requirement in semiconductor fabs is clean room production environments. Since the structures imprinted on chips measure some 40 times less than the width of a human hair, special requirements for atmospheric conditions in the production area must be met. Therefore, production equipment needs to be located in clean rooms where temperature, humidity and particle density are constant. Currently, clean rooms of class 1 are used for chip production. (See slide 11, degrees of purity). Very often, clean rooms house all the expensive production equipment and are surrounded by media supply, auxiliary units and ventilation systems. In most cases, those facilities have to be considered one fire section because of the lack of fire walls, thus bringing the maximum

possible loss amount close to the sum insured.

Main hazards
One dust particle of 0,5 µm can destroy a chip

Main hazards					
Degress of purity		Particles per cubic foot			
VDI	US Fed 209b	0,02 µm	0,1 µm	0,5 µm	5 µm
0	0,1	10^{2}	3 x 10^{o}	10-^{1}	*****
1	1	10^{3}	3 x 10^{1}	10^{o}	****
2	10	10 4	3 x 10^{2}	10^{1}	****
3	100	****	3 x 10^{3}	10^{2}	****
4	1 000	****	****	10^{3}	7 x 10^{o}
5	10 000	****	****	10 4	7 x 10^{1}

top of main document

Loss Experience

1. Operational Phase
2. Construction and Erection Phase

For various reasons, only limited statistical information on loss figures, particularly for the construction and erection phase of semiconductor fabs, is available.

- Proprietary nature of industry. All aspects, including losses, are considered production secrets and fuel the competitiveness of every fab. Therefore, no figures are provided for public use and insureds are rather reluctant to disclose detailed loss

information.

- Insurance programs for captives. There is a trend towards insurance programs covering all the activities of one particular insured. These programs provide cover for all assets in operation but, increasingly, also provide coverage for the build up of new facilities. Therefore, separate statistics for the construction and erection of fabs are not available.
- Non proportional placement of reinsurance covers. Due to the fragmentation of the placements in the reinsurance market, amassing comprehensive statistics is rather difficult.

Because of the lack of adequate statistics and rapid changes in technology, insurers tend to underestimate the daunting financial exposure they face when insuring the semiconductor industry. Total number of losses in the semiconductor industry amounted to approximately USD 60 Million for the period 1974 to 1986. For the period 1986 to 1998, the figure increased 17 fold to USD 1 Billion!

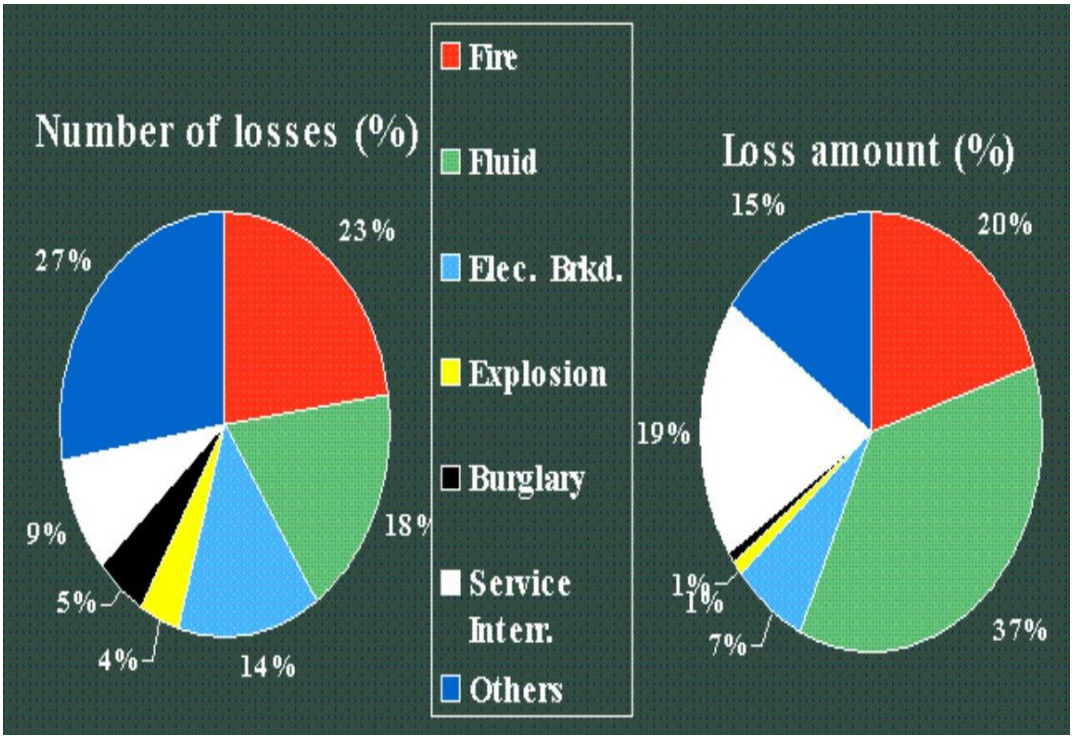
The experience gained during operation of semiconductor fabs is remarkably different from that made during the construction and erection phase of these plants.

top of main document

1. Operational Phase

Statistics available for the operational phase (see slide 12) show that most of the losses in numbers are caused by fire, followed by damages caused by liquids (including sprinkler leakage) followed by service interruption. When examining loss amounts, the picture looks quite different. There, it is evident that liquids caused the largest losses.

Loss experience 1986 to 1995, Operation



The following table is based on data provided by Factory Mutual Research Corporation on semiconductor industry losses for the years 1986 to 1995.

Peril type	Number of events (%)	Loss amounts (%)
Liquid damage	18	37
Fire/Explosion	27	21

Service interruption	9	19
Miscellaneous	46	23

The table clearly demonstrates that the loss potential mainly lies in the categories Liquid, Fire/Explosion and Service interruption damage accounting for a total of 80% of all loss amounts. Miscellaneous includes perils such as wind and hail, earth movement, collapse, burglary and theft.

top of Loss Experience

top of main document

2. Construction and Erection Phase

The figures for the construction and erection vary considerably from the operational phase as the build up of the plant creates completely different exposures than those faced during operation. Smoke and fire detection systems and sprinklers are often not operational and cable and pipe ducts are not properly sealed, creating an above average exposure to fire. Expensive and highly sensitive equipment must be transported, stored and installed. Erection works have to be performed in the vicinity of operating production lines, causing further restrictions for the contractors. The coordination of many specialized subcontractors working with very tight time schedules is a major challenge for the project management.

The loss record for the erection of semiconductor fabs has been extremely unsatisfactory for various reasons. The premiums paid have often been consumed by several small losses, such as shock damages to sensitive equipment and service interruption losses to existing production lines. In addition, two major fire losses in 1996 and 1997 have demonstrated the huge loss potential of the industry. Four losses are described to give an impression on the loss pattern of the semiconductor industry:

Typical loss examples:

A. Dropping of a stepper machine during installation (see slide 13)

The machine valued at USD 5 million was moved to the clean room. During unloading from an elevator, the machine suffered shock damage. While there was no visible damage, the machine had to be returned to the overseas manufacturer for the readjustment of the optical system. The loss amounted to USD 200,000 for readjustment and transport.

Loss experience
• **Dropping of a Stepper** • In house transport of a Stepper Machine • Scock during unloading of the equipment from the elevator in the fab • No visible damage but readjustment of potical system by the manufacturer in Japan • Loss of US$ 200´000 (Transport and readjustment)

Loss experience

- **Existing property claim**

- 50 t crane hits power cable of existing plant during construction of extension causiong a shutdown
- Wafers in process
- Chip packages damaged
- Machinery contaminated
- Loss US$ 1 Mio (Limit US$ 5 Mio)

B. Existing property claim (see slide 14) During the erection of an extension to an existing plant (project value close to USD 2 billion), the power supply to the plant under operation was cut. This caused the production process to stop. The owner of the plant claimed that the unplanned interruption had caused damage to wafers and chip packages and had also contaminated machinery. The EAR policy provided cover for "existing property" with a sub-limit of USD 5 million. The loss was finally settled at USD 1 million.

C. Fire loss (see slides 15 and 16) During the erection of a semiconductor fab, a chemical vapor deposition (CVD) machine located in a support area to a clean room caught fire. The fire devastated large areas in the support area, and smoke - as well as corrosive gases - entered the clean room. Part of the loss was indemnified by the property policy as some of the equipment had already been handed over. A major difficulty was the correct allocation of losses to the erection and the property policy as the large number of individual equipment rendered the clear identification rather complex. As large amounts of expensive production equipment were affected by chemically aggressive gases and deposits, the rapid and effective decontamination proved to be of utmost importance.

The loss was settled at an amount equivalent to USD 180 million (55% Property, 45% Engineering cover).

Loss experience

- **Winbond Fire Loss, October 1996**

- NT $ 6 Bio (US$ 180 Mio) for EAR (45%) and Property (55%)
- Fire in a CVD Machine
- Damage to support area
- Contamination of equipment in the clean room

Loss experience

Winbond Fire Loss, 14th October 1996

D. Fire Loss (see slides 17 to 19) During the replacement of parts of the acid toxic exhaust pipe ducts made of polypropylene, a fire broke out and could not be brought under control. The flames spread to other floors via the exhaust system and severely damaged supporting, as well as production areas. This incident was the most expensive single loss in the semiconductor industry to date. The loss amount of USD 350 million was split and allocated 75% to Property and 25% to Engineering covers according to the values of the equipment handed over from construction to operational covers. In this case, repair works within an operational plant were carried out. Important to note is that the fire-fighting operation was further complicated by the reluctance of the fire brigade to enter a building containing large quantities of highly explosive and toxic substances.

Loss experience

- **UICC Fire Loss, October 1997**

- NT $ 10 Bio (US$ 350 Mio) for EAR (25%) and Property (75%)
- Fire during repair work on polypropylene pipes spreading to other areas via the exhaust7ventilation system
- Severe fire damage to all areas of the plant

Loss experience

UICC Fire Loss, 3rd October 1997

Loss experience

UICC Fire Loss, 3rd October 1997

These examples clearly show the huge loss potential and highly complex loss mitigation and settlement procedures inherent to the semiconductor industry. Important to note is that the two large fire losses were for property damage only, as there was no business interruption cover in place.

top of Loss Experience

top of main document

Insurance aspects

The factors inherent to the semiconductor industry (high value concentration, rapidly changing technology, dangerous operating media, susceptibility to damage and exposure to natural perils) clearly create a well above-average exposure to Engineering and Property insurers (see slide 20).

Insurance aspects
• **Main exposures (engineering and property related:)** • Liquids (Water, other media) • Fire • Interruption of services • Shock, Transport of equipment • Explosion 8aggressive chemicals) • EQ

Insurance aspects
• **Crucial points:** • Rapidly changing technoligy • Value concentration, MPL • Susceptibility to damage • project, Risk management • Saftey, Precaution measures

Traditional pricing methods may not result in adequate terms for insurance covers for this industry. Sound project and risk management procedures are of paramount importance. The enormous complexity (see slide 21) and the huge values which hallmark this industry mean that even minor events can - and do - result in catastrophic losses. Therefore, proper project management with due reference to the particular exposures is essential. An effective risk management has to kick in at an early stage of the planning, and design of the project has to consider likely future extensions or modifications. Involving risk managers from the insured's as well as from the insurer's side early on is key to ensuring effective cooperation. The consideration of local as well as international standards in respect of protection and safety measures must be implemented from the design stage and continuously monitored, reviewed and adapted where necessary. Whenever possible, the use of combustible material (Polypropylene PP, Polyvinylchloride PVC) for ducts should be avoided. It should be noted that, in certain countries, the use of PP/PVC for ducts is already prohibited! In case combustible material is used for pipes and ducts, these should be sprinkled as well.

The insurance conditions must emphasize a sound project management, specifying adequate conditions for safety precaution and protection measures, hot work permits, and testing and hand-over procedures (see slide 22), to name but a few.

Insurance aspects
• Fire protection, sprinkler systems in clean room and ventilation ducts • Transfer of EAR to Operational covers

- Loss settlement procedures
- XS reflecting high cost of repair
- Exposure realted rate

Sprinkler systems need to be installed in clean rooms as well as in exhaust and ventilation ducts. They have to be ready for use before the installation of expensive production equipment in the clean room starts. Production equipment such as wet benches need to be equipped with separate fire detection and fighting systems. The allocation of the equipment to construction and operational insurance covers during the complex testing and hand over period has to be precisely defined in order to avoid disputes in case of a loss. In case maintenance covers are granted under Construction/Erection policies, the perils of fire and explosion should be explicitly excluded. Because of the huge fire loss potential, this peril has to be covered by the operational insurance program.

Loss settlement procedures (e.g. the use of a professional loss mitigation expert) should be clearly described prior to the issuance of the policy to avoid unpleasant and time-consuming discussions during the loss settlement process.

Excess levels for covers need to reflect the highly costly repairs for hi-tech equipment. They should be chosen to cut out the high-frequency losses eroding the premium reserves for the larger losses.

Rate levels have to reflect both the exposure and quality of the plant and those of the risk management procedures in place. The often neglected exposure towards natural perils (earthquake, storm, flood) should be considered with due care. Remember, a large number of plants are located in earthquake, as well as storm and typhoon exposed areas. To date, natural perils have not affected loss statistics heavily, but in view of the value concentration in countries with a considerable loss potential emanating from natural perils, exposures can not be neglected. These facors as well as the adverse loss experience of the recent past have to be considered when rate levels are determined.

When granting business interruption covers, utmost care must be taken. Loss settlement here, namely, is even more challenging in view of rapidly changing market conditions.

top of main document

Conclusions

Conclusions

- **Keep up with**

- High pace
- New technologies
- Risk management
- Adequate covers

The semiconductor industry is truly a special one in many respects (see slide 23, new generation of 12 inch "Pizza" wafers). Collectively, the high pace of technological development, the huge value accumulation, the susceptibility to damage and a multitude of different exposures create a challenging mix for project managers, as well as for the insurance industry. Assessing projects requires a thorough understanding of these specific exposures, and the development of adequate insurance terms can only be achieved if risk managers from the semiconductor and the insurance industries cooperate closely.

Only a professional management of the highly complex risks inherent to the semiconductor industry can provide a successful build up and safe operation of semiconductor fabs. Yet, even the most professional risk management and the implementation of state-of-the-art precautionary measures can not deter the occurrence of catastrophic losses. Therefore, the insurance cover provided should clearly address and define crucial elements - such as testing and hand-over procedures - and has to
include warranties in respect of precautionary and safety measures. The levels of excess should reflect the high repair costs incurred for minor damages, and the premium level has to consider the industry's large loss potential.

Rather than disappear in general property insurance programs, semiconductor fabs should be covered by tailor-made insurance concepts, which include adequate risk management procedures. The adverse loss experience of this type of industry only stands to be improved if insurance terms reflect the specific exposures encountered.

top of main document

back to Paper Published